

**What is claimed is:**

1           1.    An insulating device for system on chip (SOC),  
2           wherein the SOC has a first circuit region powered by a main  
3           power source and a second circuit region powered by a real-time  
4           power source, comprising:

5           a selector designating the main power source or a battery  
6           source as the real-time power source;

7           a level detector powered by operating power source to  
8           detect a voltage level of the main power source and  
9           output a resulting signal;

10          a NAND gate coupled to the first circuit and the level  
11          detector to produce a logic output according to the  
12          resulting signal and an output signal of the first  
13          circuit, wherein the NAND gate comprises:

14          a first NMOS transistor having a gate coupled to  
15          the output signal of the first circuit, and  
16          a source coupled to ground and a drain;

17          a second NMOS transistor having a gate coupled to  
18          the result signal, a source coupled to the  
19          drain of the first NMOS transistor and a drain  
20          as an output terminal;

21          a first PMOS transistor having a gate coupled to  
22          the gate of the first NMOS transistor, a  
23          source coupled the real-time power source and  
24          a drain coupled to the drain of the second NMOS  
25          transistor; and

26          a second PMOS transistor having a gate coupled to  
27          the gate of the second NMOS transistor, a  
28          source coupled to the real-time power source

29                   and a drain coupled to the drain of the second  
30                   NMOS transistor.

1           2.    The insulating device as claimed in Claim 1, further  
2           comprising an inversion gate having an input coupled to the  
3           drain of the second NMOS transistor to invert the logic output  
4           produced by the NAND gate.

1           3.    The insulating device as claimed in Claim 1,  
2           wherein, in normal operating mode, the main power source is  
3           designated as the real-time power source, such that the first  
4           circuit, the level detector and the power insulator are  
5           powered by the main power source.

1           4.    The insulating device as claimed in Claim 3,  
2           wherein, in power-down mode, the battery source is designated  
3           as the real-time power, and the first circuit is not powered  
4           by the main power source.

1           5.    The insulating device as claimed in Claim 4, wherein  
2           the resulting signal is connected to the gates of the first  
3           NMOS transistor and the first PMOS transistor without any  
4           buffer, and the output signal of the first circuit is connected  
5           to the gates of the second NMOS transistor and the second PMOS  
6           transistor without any buffer.

1           6.    An insulating device for system on chip (SOC),  
2           wherein the SOC has a first circuit region powered by a main  
3           power source and a second circuit region powered by a real-time  
4           power source, comprising:

5           a selector designating the main power source or a battery  
6           source as a real-time power source;

a level detector powered by the real-time power source  
to detect a voltage level of the main power source  
and output a resulting signal;

a NOR gate coupled to the first circuit and the level  
detector to produce a logic output according to the  
resulting signal and an output signal of the first  
circuit, wherein the NOR gate comprises:

a first PMOS transistor having a gate coupled to  
the output signal of the first circuit, a  
source coupled to real-time power source and  
a drain;

a second PMOS transistor having a gate coupled to  
the resulting signal, a source coupled to the  
real-time power source and a drain as an  
output terminal;

a first NMOS transistor having a gate coupled to  
the gate of the first PMOS transistor, a  
source coupled to ground and a drain coupled  
to the drain of the second PMOS transistor;  
and

a second NMOS transistor having a gate coupled to  
the gate of the second PMOS transistor, a  
source coupled to the ground and a drain  
coupled to the drain of the second PMOS  
transistor.

7. The insulating device as claimed in Claim 6, further  
comprising an inversion gate having an input coupled to the  
drain of the second PMOS transistor to invert the logic output  
produced by the NOR gate.

1           8.    The insulating device as claimed in Claim 6,  
2           wherein, in normal operating mode, the main power source is  
3           designated as the real-time power, such that the first  
4           circuit, the level detector and the power insulator are  
5           powered by the main power source.

1           9.    The insulating device as claimed in Claim 6,  
2           wherein, in power-down mode, the battery source is designated  
3           as the real-time power source, and the first circuit is not  
4           powered by the main power source.

1           10.   The a insulating device as claimed in Claim 6,  
2           wherein the resulting signal is connected to the gates of the  
3           first NMOS transistor and the first PMOS transistor without  
4           through buffer, and the output signal of the first circuit  
5           is connected to the gates of the second NMOS transistor and  
6           the second PMOS transistor without any buffer.